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Self-Heating and Cooling of Active Plasmonic Waveguides

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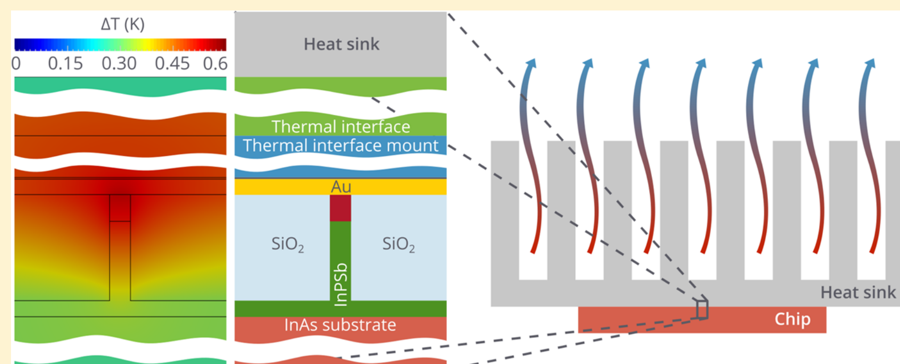
Supporting Information



ABSTRACT: Loss compensation in plasmonic nanostructures gives a possibility to avoid problems with strong absorption in the metal and design deep-subwavelength optical components for practical applications. At the same time, pumping required for creation of population inversion produces a huge amount of waste heat, which can significantly increase the device temperature and degrade its performance. Eventually, self-heating is becoming a severe problem for active plasmonics, since it limits the maximum achievable optical gain. Here we report a comprehensive study of heat generation and transport in electrically pumped active plasmonic waveguides, in which the SPP propagation losses are compensated by gain in the adjacent semiconductor and present a strategy for their efficient cooling.

KEYWORDS: *heat transport, active plasmonics, surface plasmon amplification, electrical pumping, self-heating, temperature control*

Surface plasmon polaritons (SPPs), which are surface electromagnetic waves propagating at the interface between a metal and a dielectric, can provide deep-subwavelength confinement of optical modes and give a possibility to reduce the size of photonic components down to that of electronic ones.[1−5] This makes plasmonics a prospective platform for the next generation of highly integrated optoelectronic circuits.[6,7] However, the ability to get over the diffraction limit comes at a cost of high signal attenuation due to strong absorption in the metal. This limits the SPP propagation length to several tens of micrometers in strongly confined plasmonic waveguides.[1−5] In order to increase the SPP propagation length and maintain strong mode confinement, a loss compensation scheme must be developed, where ohmic losses in the metal are compensated by optical gain in the adjacent medium.

In recent years, intensive research efforts have been focused on SPP amplification and several approaches have been proposed.[8−10] The most practically important among them are methods based on efficient and compact electrical pumping,[11−13] which is easily integrated on a chip and gives a possibility to design nanoscale plasmonic integrated circuits.[14,15] However, the injection current densities in such devices are of the order of[13,14,16] 10 kA/cm^2. This is higher than in most semiconductor laser diodes,[17] and consequently, electrically pumped active plasmonic structures may suffer from the same self-heating problem arising due to nonradiative carrier recombination, Joule and thermoelectric Peltier effects,[18,19] as semiconductor lasers. In the regimes of full loss compensation and net SPP amplification, which are of great importance in plasmonic devices, high pump currents produce a large amount of waste heat, which can substantially increase the device temperature. Accordingly, the material gain in the active medium decreases and a higher injection current is required to maintain the same modal gain (see Figure S1 in Supporting Information). This does not only reduce the net energy efficiency, but also further increases the operation temperature, which can eventually damage the device before the regime of full loss compensation is achieved.

In this article, we present for the first time an analysis of heat generation and transport in active plasmonic nanostructures. We examine heating mechanisms and show that high heat generation produced by injection currents in electrically pumped active plasmonic waveguides, where the SPP propagation losses are compensated by gain in the adjacent semiconductor, can easily increase the device temperature by more than 100 K. This makes efficient heat removal crucially important for device operation. We further numerically demonstrate that conventional cooling systems with accurately designed thermal interfaces can decrease the temperature rise

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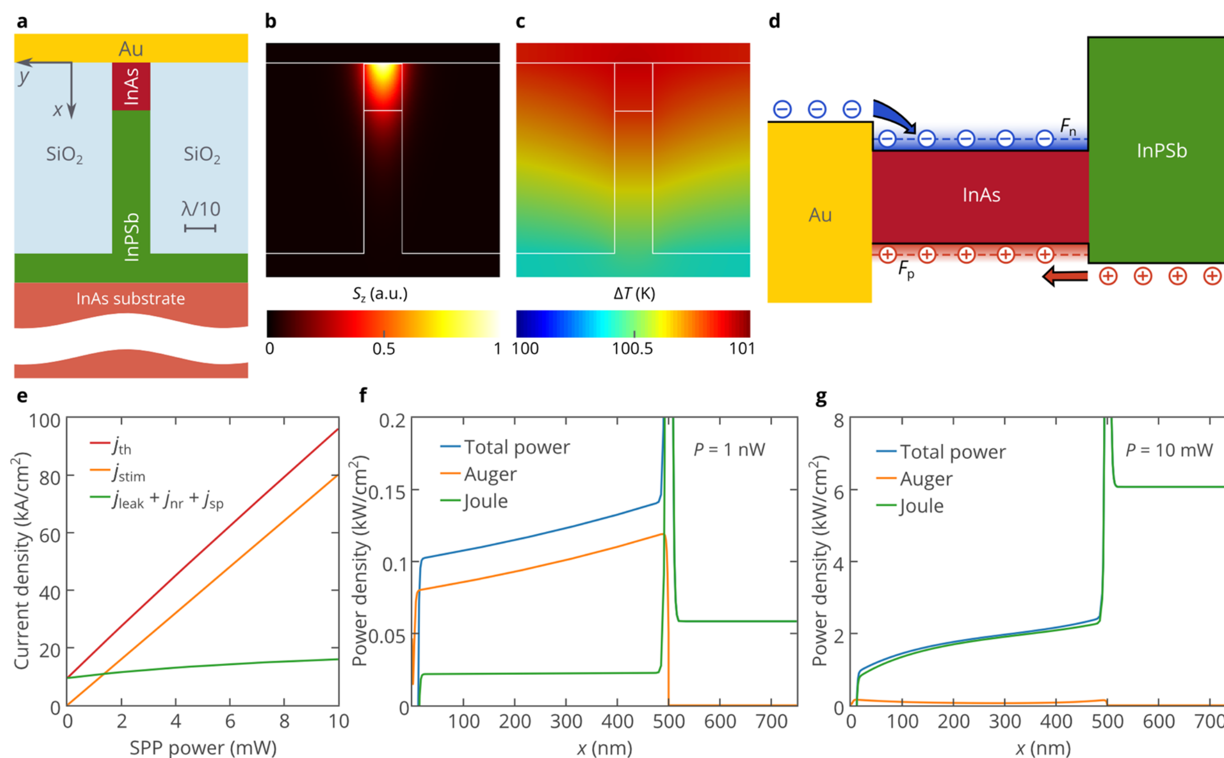

Figure 1. (a) Schematic of the electrically pumped active T-shaped plasmonic waveguide on a 150 μm thick InAs wafer, the semiconductor rib is 400 nm wide and 2 μm high, the gold layer is 300 nm thick. The active InAs region is 500 nm high and is p-type doped with an acceptor concentration of 2×10^{18} cm^{-3}. The doping level of the $InP_{0.69}Sb_{0.31}$ layer lattice matched to InAs is slightly lower and equals 1.13×10^{18} cm^{-3}. (b) Spatial distribution of the power flow of the fundamental plasmonic mode at a free space wavelength of 3.26 μm ($\hbar\omega$ = 380 meV), which corresponds to the maximum of the InAs material gain spectrum at 77 K (see Methods). The dielectric functions of the materials are as follows: $\varepsilon_{SiO_2} = 2.00$,[25] $\varepsilon_{InPSb} = 11.48$,[26] $\varepsilon_{InAs} = 12.38$,[26] $\varepsilon_{Au} = -558 + 30i$.[14] Without material gain in the semiconductor, the SPP modal loss equals 127 cm^{-1}, which includes the radiation loss of[27] 34 cm^{-1}. (c) Temperature distribution in the waveguide cross-section simulated in the regime of full loss compensation at a small SPP power $P <$ 1 nW. $\Delta T = T - T_{amb}$ is the temperature rise with respect to the ambient temperature T_{amb}. The surface heat transfer coefficient is assumed to be equal to $h = 10^{-3}$ W/(cm^{2}K) that is typical for natural air convection.[28] (d) Qualitative energy band diagram of the Au/InAs/$InP_{0.69}Sb_{0.31}$ structure in the regime of full loss compensation. The energy distance between quasi-Fermi levels for electrons (F_n) and holes (F_p) is greater than the bandgap energy of InAs, which is required for net stimulated emission in InAs.[29] (e) The pump currents as functions of the SPP power in the regime of full loss compensation: j_{stim}, j_{sp}, and j_{nr} are the current densities for the stimulated emission, spontaneous emission and Auger recombination, j_{leak} is the leakage current and $j_{th} = j_{stim} + j_{sp} + j_{nr} + j_{leak}$ is the threshold current density. (f, g) Spatial distribution of the heating power density in the regime of full loss compensation at a low (f) and high (g) SPP power, x = 0 corresponds to the Au/InAs contact. The heating power density is given per unit length per unit height of the waveguide. The temperature of the Au/InAs contact is equal to 77 K for all panels.

to a few Kelvin and allow to avoid overheating of active plasmonic nanostructures.

■ RESULTS AND DISCUSSION

Figure 1a shows a schematic of the electrically pumped T-shaped active plasmonic waveguide, which is based on a single-heterostructure Schottky-barrier diode.[14] Since InAs is one of the few semiconductor materials that form rectifying Schottky contacts to gold with a barrier height of greater than the bandgap energy of the semiconductor,[20,21] the SPP supporting metal/semiconductor interface can also be used as an electrical contact for direct injection of minority carriers into the active InAs region.[14,22] This approach gives a possibility to minimize the device footprint, which becomes limited only by the waveguide width. At the same time, thanks to the low-refractive-index SiO_2 claddings, the SPP mode propagating along the Au/InAs interface is strongly confined ($\sim\lambda/8$) in the lateral direction. The pump current flows in the vertical direction through the Au/p-InAs/$InP_{0.69}Sb_{0.31}$ Schottky-barrier single heterostructure. Under strong forward-bias conditions, high densities of nonequilibrium electrons injected from Au and holes injected from $InP_{0.69}Sb_{0.31}$ create population inversion and thus optical gain in the active InAs region of the waveguide (Figure 1c). The InAs/$InP_{0.69}Sb_{0.31}$ heterostructure serves here two purposes. First, the large bandgap $InP_{0.69}Sb_{0.31}$ material confines electrons in the InAs layer reducing leakage currents. Second, the refractive index of $InP_{0.69}Sb_{0.31}$ is lower than that of InAs, which improves the plasmonic mode confinement in the vertical direction, preventing the SPP from leaking into the substrate. Self-consistent numerical simulations (see Methods) demonstrate that, at a temperature of 77 K (which is chosen due to strong Auger recombination in InAs and is typical for mid-infrared optoelectronic devices[23,24]) and a small signal power, the current density required for full compensation of the SPP propagation losses (further referred to as the threshold current density) is as low as 9.4 kA/cm^2. But the threshold current rapidly increases as the SPP signal power P_{SPP} increases. At P_{SPP} = 10 mW, the threshold current is 1 order of magnitude higher and equals 96 kA/cm^2. Whereas at a low SPP power the injection current is dominated by the leakage current and current for the Auger recombination, stimulated emission prevails over the other processes for $P_{SPP} >$ 1 mW, which

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ACS Photonics 2016, 3, 51−57

significantly affects the carrier and currents spatial distributions. Nevertheless, even at a low signal power, the threshold current is significantly high and produces heat giving rise to the device temperature.

In order to understand the impact of self-heating on the device performance, we consider closely heat generation mechanisms and heat transport processes. Volumetric heat generation in the semiconductors is due to the Joule effect and nonradiative Auger recombination. The Joule heating power density can be found as $j\nabla\varphi$, where j is the current density and φ is the electrostatic potential, while the power density due to Auger heating is given by[30] $E_g^{InAs}(C_p p^2 n + C_n n^2 p)$, where C_n and C_p are the Auger recombination coefficients, n and p are the electron and hole densities in InAs, respectively, and E_g^{InAs} is the bandgap energy of InAs. As it can be easily seen, in each act of Auger recombination, an energy of about 0.4 eV is released and consequently the contribution of the Auger process to the total heating power can be substantially higher than that of the Joule heating (Figure 1f). In the regime of full loss compensation, the Auger heating power determined by the carrier concentrations does not appreciably depend on the SPP power, while the Joule heating power rapidly increases with the SPP power due to the increase in the pump current density and exceeds the Auger power by more than 2 orders of magnitude at P_{SPP} = 10 mW (Figure 1g).

In addition to the heat generation in the bulk of the semiconductor, heat is produced at the metal/semiconductor interface due to the thermoelectric Peltier effect and SPP ohmic losses in the metal. First, holes leaking from the active InAs region into the gold contact are not in equilibrium with the metal lattice and subsequently relax to equilibrium via phonon emission. Second, electrons injected from gold into InAs also contribute to the Peltier heat, since the energy of injected electrons is about[21] 0.13 eV greater than that of the quasi-equilibrium electrons in InAs. Accordingly, the Peltier heat generated at the Au/InAs contact is $P_{Peltier} \approx J_n(F_m - E_c) + J_p(F_m - E_v)$, where J_n and J_p are electron and hole currents through the contact, F_m is Fermi level in gold, E_c and E_v are the conduction and valence band energies of InAs at the Au/InAs contact. The similar Peltier effect produces heat at the InAs/InPSb interface. However, since the valence band offset between InAs and InPSb is as small as[20] 0.024 eV and the electron current through the InAs/InPSb heterojunction is nearly zero, the heat generation rate is more than 20× lower than at the Schottky contact. Finally, SPP absorption in the metal results in heat release in a ∼30 nm thick gold layer near the Au/InAs interface. The corresponding heat power per unit of waveguide length is equal to $P_{loss} = (1/8\pi)\int_{y<0}\omega \mathrm{Im}(\varepsilon_{Au})|E(x, y)|^2 dxdy = \alpha_{Au}P_{SPP}$, where $E(x,y)$ is the complex electric field amplitude of the SPP field and α_{Au} is the part of total SPP propagation loss attributed to absorption in the metal (the net SPP propagation loss in the passive regime is given by $\alpha_{SPP} = \alpha_{Au} + \alpha_{rad}$, where α_{rad} is ascribed to radiation losses due to leakage into the substrate).

At a low SPP power, in the regime of full loss compensation, the net volumetric heat generation per unit length of the active waveguide is as low as 8.5 mW/cm, while the contact heating power $P_{cont} = P_{Peltier} + P_{loss}$ is more than 20× higher and equals 190 mW/cm (Figure 2). Apparently, the heating power increases as the SPP power increases and reaches 3.8 W/cm at P_{SPP} = 10 mW.

It should be pointed out that the net heat generation is quite high even at a low SPP power and can give substantial rise to

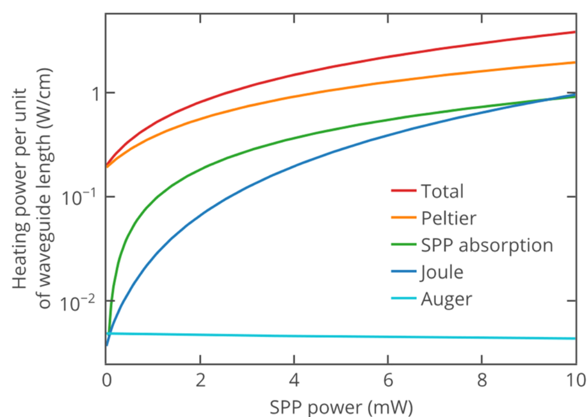

Figure 2. Dependence of the heating power and its contributions vs the SPP power in the regime of full loss compensation. The temperature of the active plasmonic waveguide is equal to 77 K.

the device temperature. Without a heat sink, the surface heat transfer coefficient can be roughly estimated as $h = 10^{-3}$ W/(K cm^2) (which is a typical value for natural air convection at standard conditions[28]), and the temperature of the single active plasmonic waveguide on an InAs wafer can be roughly evaluated as $\Delta T \approx (P_{cont} + P_{vol})/2hw_d$, where w_d is the wafer width. This simple expression demonstrates that for the 1 cm wide substrate the temperature rise is as high as 100 K, even at a very low SPP power. This estimation agrees well with the results of numerical simulations (see Methods) presented in Figure 1c. Such a high temperature increase affects the electrical properties of the semiconductors, material gain in the active region, recombination rates (includes spontaneous emission recombination and Auger recombination), and SPP loss in the metal (see Figure S1 in Supporting Information) and can decrease the device performance. At the same time, the temperature distribution across the chip is nearly uniform: the temperature of the hottest spot at the Au/InAs interface is only 1.5 K higher than that of the coolest spot of the chip, while the 100 K temperature rise is attributed to the high thermal resistance of the chip/air interface. This illustrates that the actual waveguide temperature is determined by the cooling system rather than by the nanostructure itself, and an external heat sink should be used to improve heat removal and decrease the temperature of the active region of the active plasmonic structure.

For efficient dissipation of the waste heat, the heat sink should be mounted to the chip with a high thermal conductivity layer. Tin/lead solder with a conductivity of[31] 0.5 W/(K cm) can be used to ensure a good thermal contact. Figure 3a shows the bottom-side cooling scheme: the 100 μm thick thermal interface material (solder) and 2 μm thick thermal interface mount layer (aluminum) are placed between the substrate and the heat sink. This mounting configuration minimizes risks of waveguide damage during bonding of the heat sink to the chip and is preferable in laboratory conditions. Figure 3a demonstrates drastic improvement of thermal management against the air cooling scheme. In the regime of full compensation of the SPP propagation losses, at a small SPP signal power, the temperature rise in the device structure is as low as ΔT = 2.8 K at a heat-sink thermal resistance per unit area of R_{HS} = 1 K cm^2/W, which corresponds to the thermal resistance of ordinary microprocessor heat-sink/fan assemblies.[32] As R_{HS} decreases down to 0.1 K cm^2/W (thermal

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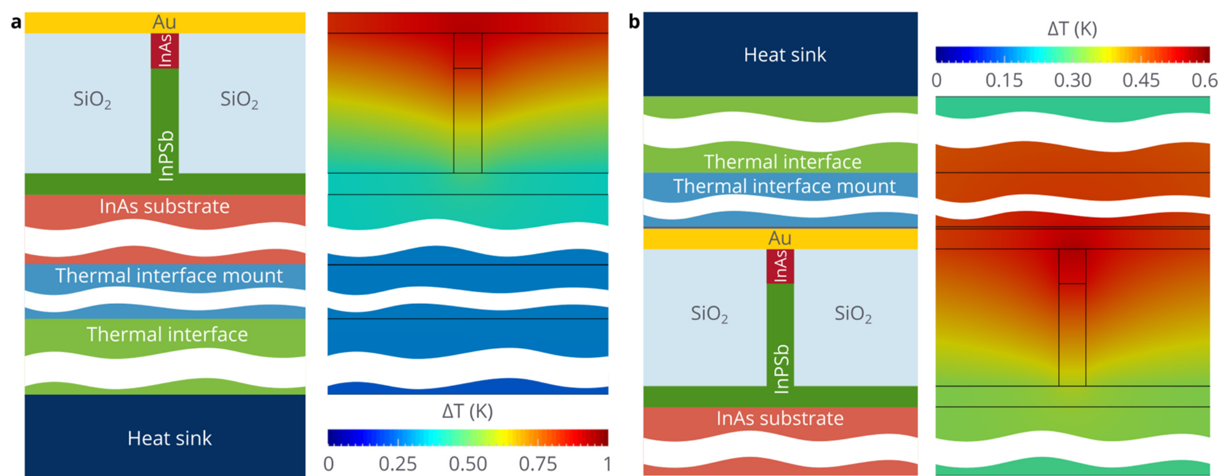

Figure 3. Bottom-side (a) and top-side (b) cooling schemes and their respective temperature profiles obtained at a small SPP signal power of P_{SPP} = 1 nW and a waveguide temperature of 77 K. The bottom-side cooling scheme consists of a 2 μm thick thermal-interface-mount layer (1 nm Ti and 2 μm Al) and 100 μm of the TIM. The top-side cooling scheme is essentially the same as the bottom-side cooling scheme, but includes an additional 30 nm-thick electrical insulating Al_2O_3 layer between Au and the thermal-interface-mount layer, which is added here to isolate the active plasmonic waveguide electrically from the heat sink and thermal interfaces. The InAs wafer is 150 μm thick and 1 mm wide and the heat-sink thermal resistance is R_{HS} = 0.1 K cm^2/W.

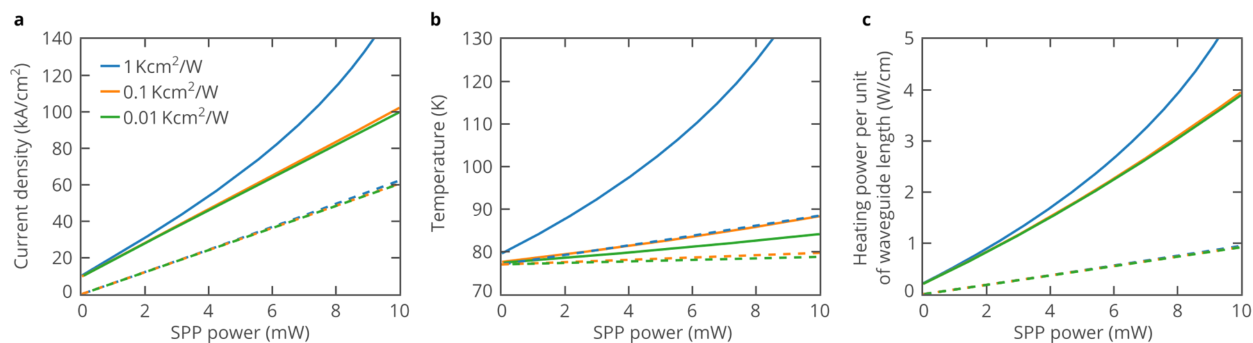

Figure 4. (a) Threshold current density vs the SPP power for different heat-sink resistances in the top-side cooling scheme: 1 K cm^2/W (heat-sink/fan assembly[32]), 0.1 K cm^2/W (typical microchannel heat sink[33,34]), 0.01 K cm^2/W (state-of-the-art CVD diamond microchannel heat sinks[37]). (b) Dependence of the temperature at the Au/InAs contact (see Figure 3b) on the SPP power in the regime of full loss compensation for the same heat resistance as in (a). (c) Heat generation per unit of the waveguide length vs the SPP power. Dashed lines correspond to the ideal compensator and the coloring schemes for them coincide with that for the single-heterostructure Schottky active plasmonic waveguide. For all panels, the ambient temperature is 77 K.

resistance of microchannel heat sinks, widely used for cooling microelectronic devices[33,34]), the temperature rise ΔT decreases to 0.9 K, most of which is attributed to the thermal resistance of the InAs substrate, thermal interface, and thermal interface mount, while the temperature at the interface between the heat sink and thermal interface is only 0.2 K above the ambient (Figure 3a).

Many applications of active plasmonic structures require them to be a part of on-chip optoelectronic circuits. Consequently, when the chip is mounted on a board, implementation of the bottom-side cooling scheme is not possible. Therefore, the heat sink should be mounted on top of the chip. Figure 3b shows the top-side cooling scheme, which is found to be even more efficient than the bottom-side scheme, since the heat generated at the metal/semiconductor contact does not pass through the bottleneck of the narrow waveguide and enters directly into the thermal interface mount layer. The temperature rise is 2.4 K at R_{HS} = 1 K cm^2/W and 0.6 K at R_{HS} = 0.1 K cm^2/W (Figure 3b).

Loss compensation in deep-subwavelength plasmonic waveguides makes them very attractive for on-chip communication.[14,35] In this case, an electrical signal is converted into an optical one and transferred in the plasmonic waveguide. Each bit of information is represented by an optical pulse of finite energy[36] and, consequently, the average SPP power can be significantly large at a high bitrate. In this regard, important is the dependence of the pump current and the temperature of the active region on the SPP signal power in the regime of full loss compensation. In Figure 4, it is clearly seen that the temperature and current characteristics almost coincide for the heat-sink resistances below 0.1 K cm^2/W, since in this case the temperature rise is mostly determined by the thermal resistances of the thermal interface and the thermal interface mount layer rather than by the heat-sink resistance. The temperature in the active region surpasses the ambient temperature by less than 11 K. At the same time, for higher R_{HS}, the temperature of the active region is governed by the high heat-sink resistance and rapidly increases with increasing P_{SPP}, which adversely affects the threshold current density (Figure 4).

In order to understand the origin of self-heating and estimate the efficiency of the considered active plasmonic structure, we

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ACS Photonics 2016, 3, 51−57

introduce here an ideal compensator, the device, which fully compensates the SPP propagation losses and dissipates the minimum possible power. As discussed above, the net injection pump current in the Au/InAs/InPSb active waveguide comprises the leakage current and recombination currents (for Auger recombination, spontaneous and stimulated emission). Among them, only the current for stimulated emission is responsible for SPP amplification, while other contributions simply increase heat generation, decreasing the energy efficiency of the active plasmonic device. Hence, to design an ideal compensator, one should block the leakage current, suppress Auger recombination in the active region, and mitigate Joule and Peltier heating power by using advanced materials. Thus, the threshold current in the ideal compensator is determined only by the stimulated emission recombination and can be found as $q\alpha_{SPP}P_{SPP}/\hbar\omega$. At the same time, in the ideal compensator, it is impossible to eliminate SPP absorption in the metal, which will remain the sole source of heat.

The concept of an ideal compensator gives a possibility to establish the fundamental limit imposed by self-heating of active plasmonic nanostructures. As seen in Figure 4c, SPP absorption in the metal contributes significantly to the net heat generation in the structure and up to 25% of the temperature rise is attributed to this effect at high SPP powers. At the same time, in Figure 4a, the slopes of the curves for the active SPP waveguide and ideal compensator are almost the same, which is a sign of the high differential efficiency $\eta_{diff} = \alpha_{SPP}q/\hbar\omega \times dP_{SPP}/dJ$ of the active plasmonic waveguide (η_{diff} is from 81 to 96%, depending on the bias voltage and heat-sink thermal resistance). In other words, parasitic currents do not increase appreciably with the increase of the SPP power and the corresponding temperature rise. This is a key factor, which minimizes the self-heating problem and ensures high energy efficiency of the loss compensation scheme in high power regimes, which are important for the nanolaser design,[22,38,39] although heat dissipation in that case is more efficient compared to the considered 2D geometry due to the small longitudinal size of plasmonic cavities.

CONCLUSION

To summarize, it has been shown that, at high pump currents required for compensation of the SPP propagation losses in deep-subwavelength plasmonic waveguides, a large amount of waste heat is released and therefore efficient thermal management is crucial for device operation. The temperature rise in the active SPP waveguide on a semiconductor wafer exceeds 100 K in atmosphere. At the same time, the temperature distribution in the waveguide cross-section is nearly uniform, and the temperature rise is determined by the macroscopic cooling scheme rather than by the nanostructure itself. We have demonstrated that self-heating can be significantly reduced by using conventional cooling systems along with a properly designed thermal interface, which give a possibility to decrease the temperature rise down to a few Kelvin at small and moderate SPP powers. As the SPP power increases, the waveguide temperature increases. Remarkable is that up to 25% of the temperature rise is attributed to the unavoidable heat generation in the metal due to SPP absorption. At the same time, heating can be virtually avoided at practical values of the SPP power. For example, considering lossless plasmonic waveguides for on-chip optical interconnects,[14,15,35] each bit of information is represented by an optical pulse with an energy of[36,40] ~1 fJ and accordingly an averaged SPP power is as small as ~50 μW at a bit rate of 100 Gbit/s. This leads to the temperature rise of less than 2.8 K, as can be seen from Figure 4b. We finally note that in large-scale highly integrated circuits the temperature rise can be an order of magnitude higher due to the large density of waveguides per unit area. However, this will not significantly decrease the waveguide performance thanks to the high differential efficiency of the amplification scheme.

METHODS

Material Gain in InAs. Material gain in heavily doped p-type InAs due to band-to-band optical transitions is calculated using Stern's model.[41−43] This approach accounts band tails in the density of states of the conduction and valence bands arising due to heavy doping effects. We also take into consideration bandgap narrowing with an increase of the acceptor concentration.[44]

Modal Gain. Modal gain of the highly confined SPP mode is related to the material gain $g(x,y)$ in the InAs active region as[45]

$$G = \frac{cn_{InAs}\int_{\Omega_{InAs}} g(x, y)|E(x, y)|^2 dxdy}{8\pi\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} S_z(x, y)dxdy} - \alpha_{SPP} \quad (1)$$

where integration in the numerator is performed over the active InAs region, n_{InAs} is the real part of the refractive index of InAs, $E(x,y)$ is the complex amplitude of the SPP electric field, and $S_z(x,y)$ denotes the z-component of the Poynting vector and α_{SPP} is the SPP modal loss without gain in the active region.

Optoelectronic Simulations. We have used the self-consistent steady-state electro-optical model,[14] which comprises Poisson's equation for the electric field and carrier densities, semiconductor drift-diffusion equations for electrons, and holes and carrier continuity equations. The latter connect electrical and optical properties of the structure and include spontaneous emission enhanced by the Purcell effect and stimulated emission, which introduces implicitly the SPP power into equations. These differential equations supplemented with 12 boundary conditions at the heterojunction and contacts are solved using the finite-difference method on a nonuniform mesh, which is fine near the metal−semiconductor contact and heterojunction and coarse in the remaining areas.

Thermal Analysis. Heat transport in the active plasmonic structure has been simulated using the 2D finite element method[46] for the nonlinear stationary heat equation

$$\nabla(\kappa(T)\nabla T) = Q \quad (2)$$

Here, $\kappa(T)$ is the temperature-dependent thermal conductivity and Q is the volumetric heat power density. At the material interface, the heat flux is continuous, however the heat release P_{cont} at the Au/InAs interface leads to the temperature gradient discontinuity at the material boundary. Weak variational form of the heat equation gives a possibility to treat this contact heat by adding a surface integral over the interface into variational form

$$\int\kappa(T)\nabla T\nabla\nu dV - \int_{Au-InAs} P_{cont}\nu dS = \int Q\nu dV \quad (3)$$

where ν is the test function. To simulate the finite thermal resistance of the heat sink, we use the Robin boundary condition $\kappa(T)\nabla T = \Delta T|_{HS}/R_{HS}$ at the boundary between the heat sink and the thermal interface, where R_{HS} is the heat-sink

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ACS Photonics 2016, 3, 51−57

thermal resistance per unit area and $\Delta T|_{HS}$ is the temperature difference between the environment and point at the heat-sink surface. Since the convective heat transfer coefficient of air is more than 3 orders of magnitude lower than the heat transfer coefficient in the presence of the worst heat sink, we neglect heat dissipation through the lateral sides of the structure, where the heat sink is not in contact with the chip surface, and apply natural boundary conditions there. Finally, the thermal model is coupled to the optoelectronic model with the spatial distribution of the volumetric (Q) and surface (P_{cont}) heat power densities. At the same time, in the optoelectronic model we introduce the temperature dependence of the bandgap energy,[47] recombination constants and carrier mobilities (for details, see Figure S1 in Supporting Information).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsphotonics.5b00449.

Temperature dependences of basic electro-optical properties (PDF).

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Notes

The authors declare no competing financial interest.

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